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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application No.:	09/896,573
Applicant:	Yoshio HAGIHARA
For:	SOLID-STATE IMAGE-SENSING DEVICE
Confirmation No.:	7850
Customer No.:	24367
Docket No.:	15162/03810
Filed:	June 29, 2001
Group Art Unit:	2878
Examiner:	Stephone B. Allen

MS APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

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April 22, 2004
Date of Deposit

Brian E. Harris
Name of Applicant, Assignee, or Registered Representative

Signature

April 22, 2004
Date of Signature

BRIEF ON APPEAL

This Brief is submitted in triplicate.

Real Party in Interest

The real party in interest in the present Application is Minolta Co., Ltd.

Related Appeals and Interferences

There are no related appeals or declared interferences which will directly affect or be directly affected by the present Application to the knowledge of the undersigned.

Status of Claims

Claims 1-23 are the subject of this appeal. No other claims are pending.

Status of Amendments

No amendments were made to the application by Appellant in response to the Office Action of September 8, 2003.

Summary of Invention

An embodiment of an image sensing device according to the present invention is shown in Figure 1. The image sensing device includes ordinary pixels G1n through Gm1 and compensation pixels G10 through Gm0. Figures 3, 7, 9, and 12 show examples of ordinary pixels, and Figures 4-7, 8, 10, 11, 13, and 14 show examples of compensation pixels. The image sensing device shown in Figure 1 is exemplified in independent claims 1, 15, 16, and 21. For example, each of claims 1 and 15 recites a solid-state image-sensing device that includes a first pixel that can generate a signal proportional to an amount of incident light (i.e., ordinary pixel) and a second pixel that can generate a compensation signal for compensating the output of the first pixel (i.e., compensation pixel).

The specification, at paragraphs 13-32, provides a detailed description of the operation of the image sensing device shown in Figure 1. In summary, each column of pixels (e.g., pixels G10 through G1n) includes a compensation pixel (e.g., G10) and a plurality of ordinary (light-sensing) pixels (e.g., G11 through G1n). The compensation pixel G10 outputs compensation data for compensating the image data output from each of

the ordinary pixels G11 through G1n. A line memory 10 is provided for storing the compensation signal so it can be used repeatedly for compensating the image data from each of the ordinary pixels G11 through G1n. A differential amplifier 11 receives, at the non-inverting input, image data from one of the ordinary pixels G11 through G1n and receives, at the inverting input, compensation data from the line memory 10. The differential amplifier 11 then outputs compensated image data, which is the inputted image data minus the inputted compensation data.

As mentioned above, the specification provides several examples of ordinary pixels and compensation pixels. For example, paragraphs 34-37 discuss in detail a first embodiment of an ordinary pixel shown in Fig. 3, and paragraphs 38-43 discuss in detail a first embodiment, first example compensation pixel shown in Fig. 4. However, for purposes of the present appeal, a detailed description of the pixel circuitry is unnecessary. Thus, the present discussion will be limited to aspects of the disclosed pixels specifically addressed by the pending claims.

A first embodiment of an ordinary (light-sensing) pixel is shown in Fig. 3, and three examples of compensating pixels for use with the first embodiment of an ordinary pixel are shown in Figs. 4-6. In the ordinary pixel shown in Fig. 3, photodiode PD and transistor T1 together constitute an embodiment of a photoelectric conversion circuit and transistors T2 and T3 together constitute an output amplifier circuit. (Specification, paragraph 34, lines 10-11). A signal is output to signal line 5 via transistor T3 according to an amount of light incident on photodiode PD. (Specification, paragraph 36, lines 2-5). More specifically, the transistors T1 and T2 are operated in the subthreshold region so the output to signal line 5 is natural-logarithmically proportional to the amount of light incident on photodiode PD. (Specification, paragraphs 35 and 36).

The compensation pixel shown in Fig. 4 is essentially the pixel shown in Fig. 3 with an additional transistor T4. A direct-current voltage VD is fed to the source of

transistor T4. Thus, the signal output to signal line 5 via transistor T3 is commensurate with the voltage VD. (Specification, paragraph 41, lines 2-5).

Figs. 5 and 6 show alternative examples of compensation pixels for use with the first embodiment of an ordinary pixel. Most notable is the example shown in Fig. 6, where the photodiode PD and transistor T1 have been eliminated. It will be appreciated that the compensation pixel of Fig. 6 outputs a signal commensurate with a voltage VD supplied to transisitor T4. However, since the photodiode PD and transistor T1 are eliminated, the compensation pixel of Fig. 6 is simpler in configuration and smaller in size than the ordinary pixel of Fig. 3. (Specification, paragraph 54, lines 3-7).

Fig. 7 shows a second embodiment of an ordinary pixel. It will be noted that the pixel shown in Fig. 7 is similar to the compensation pixel shown in Fig. 4. However, a notable difference is that the pixel shown in Fig. 7 receives a binary signal ϕVPS at the source of transistor T1 as opposed to the direct-current voltage VPS provided to transistor T1 in the first embodiment. The signal ϕVPS allows the pixel to be controlled to output a signal that is either natural-logarithmically or linearly proportional to the amount of light incident on the photodiode PD. (Specification, paragraph 58). More specifically, by varying the voltage level to the source of transistor T1, the transistors T1 and T2 can be controlled to operate in the subthreshold region or not. (Specification, paragraph 57, lines 5-7). When the signal ϕVPS is low, the transistors T1 and T2 operate in the subthreshold region, so the output signal to signal line 5 is natural-logarithmically proportional to the amount of light incident on photodiode PD. (Specification, paragraphs 59-61). When the signal ϕVPS is high, the transistors T1 and T2 are brought out of the subthreshold region, so the output signal to signal line 5 is linearly proportional to the amount of incident light. (Specification, paragraphs 63 and 64).

Another feature of the pixel shown in Fig. 7 is that, since it includes the transistor T4 like the compensation pixel shown in Fig. 4, it can be used as an ordinary pixel or as a compensation pixel. (Specification, paragraph 66).

Issue

The sole issue is whether claims 1-23 are patentable under 35 U.S.C. § 103(a) over U.S. Patent No. 6,191,408 to Shinotsuka et al. ("Shinotsuka") in view of U.S. Patent No. 6,133,862 to Dhuse et al. ("Dhuse").

Grouping of Claims

In order to make the appeal process as efficient as possible and for the purpose of this Appeal only, Appellants agree to have the claims of the sole issue considered in a single group.

Argument

Sole Issue – Whether claims 1-23 are patentable under 35 U.S.C. § 102(e) over Shinotsuka in view of Dhuse.

Claims 1-23 include independent claims 1, 15, 16, and 21, wherein claims 2-14 depend, directly or indirectly, from claim 1, claims 17-20 depend, directly or indirectly, from claim 16, and claims 22 and 23 depend from claim 21.

With respect to claim 1, this claim recites:

> A solid-state image-sensing device comprising:
> a first pixel including a photoelectric conversion element and capable of generating an output signal that is logarithmically proportional to an amount of light incident on the photoelectric conversion element;
> a second pixel for generating as an output signal a compensation signal with which to compensate the output signal of the first pixel; and
> a reading circuit for reading out the output signals of the first and second pixels.

Thus, claim 1 relates to a solid-state image-sensing device comprising two pixels, where one of the pixels generates a signal to compensate a signal from the other pixel, as well as a reading circuit for reading the signals from the two pixels.

With respect to the other independent claims, independent claim 15 recites a first and second pixel, where the second pixel generates "a compensation signal with which to compensate the output signal of the first pixel," independent claim 16 recites a first and second pixel, where the second pixel "is used for reducing noise that is caused by the first pixel," and independent claim 21 recites a first and second pixel, where the second pixel generates "a compensation signal with which to compensate for a variation ascribable to a characteristic of the reading circuit."

Shinotsuka relates to a photosensor processing apparatus 5 for receiving output voltages Vo from respective photosensors 4 of an image sensor 1. The apparatus 5 is designed to correct for variations in sensor output voltages Vo among the photosensors 4 that contribute to fixed-pattern noise (FPN). (Shinotsuka, col. 2, lines 11-21). The apparatus 5 includes a correcting device 6. As shown in Fig. 5, the correcting device 6 comprises an inflection point data storage device 7, which is a memory such as a ROM for storing a set of data V_A about respective inflection points of the photosensors 4. (Shinotsuka, col. 7, lines 1-4). The correcting device 6 also includes a reference inflection point data setting device 9, which is a memory such as a RAM for storing respective reference inflection point data that is input in advance from a data input device, such as a keyboard (reference inflection point input device 11). (Shinotsuka, col. 7, lines 19-22 and 54-57). The correcting device 6 further comprises a data comparator 8 and a calculation device 10.

Dhuse relates to an apparatus for reducing reset noise in photodiode-based sensors. Dhuse indicates that two causes of reset noise are "fluctuations in the level of Vcc and switching noise in the operation of transistor M1...." (Dhuse, col. 5, lines 10-13). Dhuse takes the approach of adding a "reference pixel" for determining and allowing for the correction of the fluctuation in the level of Vcc coming from the voltage source. (Dhuse, col. 6, lines 1-5). As can be seen by comparing Dhuse Figs. 2 and 4, wherein Fig. 2 shows a circuit for a MOS image-sensing pixel 200 and Fig. 4 shows a circuit for the reference pixel 400, the reference pixel 400 is a slight modification of the MOS image-sensing pixel

200. The basic difference, as can be seen by comparing Figs. 2 and 4, is that the reference pixel 400 has a capacitor 418 in place of a photodiode PD1 that is used in the MOS image-sensing pixel 200.

In setting forth the present rejection, the examiner alleges that "[i]t would have been obvious to one of ordinary skill in the art at the time that the invention was made to provide the correction circuitry 6 of Shinotsuka in the form of a pixel...." (September 8, 2003 Office Action, page 3, last three lines). This allegation is respectfully traversed, and it is respectfully pointed out that both Shinotsuka and Dhuse fail to teach a pixel that includes a ROM, a RAM with an input from a keyboard or the like, a comparator, and a calculation device so as to make the proposed combination obvious to one of ordinary skill in the art at the time of the present invention. As mentioned above, the reference pixel disclosed in Dhuse is a relatively minor modification of a MOS image-sensing pixel, where a photo-diode has been replaced with a capacitor. This simple modification disclosed by Dhuse is insufficient for teaching to one of ordinary skill in the art, at the time of the invention, how to incorporate all of the elements of the Shinotsuka correcting device 6 into a pixel such as the reference pixel 400 of Dhuse. It has been established that "[o]bviousness cannot be proved ...without explaining how references would teach ...[the] combination of elements in [the] patent ...." (*Aero Industries v. John Donovan Enterprises – Florida Inc.*, 53 USPQ2d 1547, 1557 (DC Sind. 1999)).

Dhuse even advises that "[i]t is ...desirable to have a method and apparatus ...using current pixel designs to achieve improved sensitivity and noise performance using electrical circuitry available with standard MOS fabrication processes." (Dhuse, col. 2, lines 30-33). While it seems reasonable to replace a diode with a capacitor in a MOS device using pixel designs at the time of the invention and standard MOS fabrication processes as is done in Dhuse, it is unreasonable to suggest that Shinotsuka and Dhuse teach implementing the Shinotsuka correcting circuit 6 into a known pixel design using some standard MOS fabrication process. Thus, Dhuse explicitly discourages, rather than motivates, the proposed combination of Shinotsuka and Dhuse.

In addition, it is maintained that the function of the reference pixel 400 disclosed in Dhuse is not the same as the function of the Shinotsuka correcting device 6. The Dhuse reference pixel 400 is for "determin[ing] the amount of noise on the power supply voltage, labeled Vcc..." (Dhuse, col. 6, lines 3-4) and "removing the row reset noise that is caused by supply voltage variations...." (Dhuse, col. 6, lines 12-13). On the other hand, the Shinotsuka correcting device 6 is for "correct[ing] [for] variations in characteristics between pixels of an image sensor...." (Shinotsuka, col. 2, line 14) that contribute to fixed-pattern noise (FPN). There is no evidence to support an allegation that one of ordinary skill in the art, given these two references that each disclose correcting for different sources of noise using different methods and different apparatuses, would be motivated to combine these references in the drastic way suggested by the examiner.

Nevertheless, the examiner alleges that the combination would be obvious "in order to consolidate the compensation and output signal elements rather than separating them, which would require more space." (September 8, 2003 Office Action page 3, last three lines – page 4, lines 1-2). The examiner further alleges that "by designating separate, second pixels to obtain a correction signal value, the correction signals applied to the first pixels would not be biased by problems inherent to the first output signal pixels." (March 7, 2003 Office Action, page 4, lines 11-13).

In response, it is first respectfully pointed out that there is no teaching in Shinotsuke or Dhuse related to either of the above statements cited from the Office Action. For example, it is unclear how, based on the teachings of Shinotsuka in view of Dhuse and the knowledge available to one of ordinary skill in the art at the time of the present invention, the proposed combination of Shinotsuke and Dhuse would result in a consolidated, smaller device when Dhuse provides no teaching related to shrinking and/or consolidating the correcting circuit 6 of Shinotsuke that functions to correct for variations in pixel characteristics between pixels of an image sensor.

It is further altogether unclear how, based on the teachings of Shinotsuka in view of Dhuse and the knowledge available to one of ordinary skill in the art at the time of the present invention, the proposed combination would result in some device wherein "the correction signals applied to the first pixels would not be biased by problems inherent to the first output signal pixels." It is also respectfully pointed out that this could not be considered a motivating factor for combining Shinotsuka and Dhuse, since the Shinotsuka correcting device 6 already receives correction signals J_I, which are not biased by problems inherent to a pixel, from the reference inflection point input device 11.

Thus, for all of the reasons discussed above, there exists no suggestion or motivation, in the references or in the knowledge generally available to one of ordinary skill in the art, to combine Shinotsuka and Dhuse. Accordingly, the proposed combination of Shinotsuke and Dhuse cannot render obvious claims 1-23.

Conclusion

In view of the foregoing, a *prima facie* case of obviousness has not been established with regard to claims 1-23. Accordingly, Appellants respectfully request the Board of Patent Appeals and Interferences to reverse the Examiner's rejections as to all of the appealed claims.

Respectfully submitted,

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APPENDIX

1. (Original) A solid-state image-sensing device comprising:

a first pixel including a photoelectric conversion element and capable of generating an output signal that is logarithmically proportional to an amount of light incident on the photoelectric conversion element;

a second pixel for generating as an output signal a compensation signal with which to compensate the output signal of the first pixel; and

a reading circuit for reading out the output signals of the first and second pixels.

2. (Original) A solid-state image-sensing device as claimed in claim 1, wherein the solid-state image-sensing device has a plurality of first pixels.

3. (Original) A solid-state image-sensing device as claimed in claim 2, wherein the solid-state image-sensing device has a plurality of second pixels.

4. (Original) A solid-state image-sensing device as claimed in claim 3, wherein the first pixels are arranged in a two-dimensional array, and the second pixels are arranged in a line in such a way as to correspond one to one to columns of the first pixels.

5. (Original) A solid-state image-sensing device as claimed in claim 4, further comprising:

a plurality of output signal lines provided one for each column of pixels, the output signal lines each permitting the output signals of the first and second pixels arranged in an identical column to be extracted therethrough.

6. (Original) A solid-state image-sensing device as claimed in claim 1, wherein the second pixel is smaller in size than the first pixel.

7. (Original) A solid-state image-sensing device as claimed in claim 1, wherein the first and second pixels have different circuit configurations.

8. (Original) A solid-state image-sensing device as claimed in claim 7, wherein, whereas the first pixel includes the photoelectric conversion element, the second pixel includes no photoelectric conversion element.

9. (Original) A solid-state image-sensing device as claimed in claim 1, wherein the first and second pixels have an identical circuit configuration.

10. (Original) A solid-state image-sensing device as claimed in claim 9, wherein the first and second pixels receive different voltages.

11. (Original) A solid-state image-sensing device as claimed in claim 1, wherein the first and second pixels each include a plurality of MOS transistors.

12. (Original) A solid-state image-sensing device as claimed in claim 1, wherein the first pixel generates selectively either the output signal that is logarithmically proportional to the amount of incident light or an output signal that is linearly proportional to the amount of incident light.

13. (Original) A solid-state image-sensing device as claimed in claim 1, further comprising:

a compensation circuit for compensating the output signal of the first pixel with the output signal of the second pixel.

14. (Original) A solid-state image-sensing device as claimed in claim 13, wherein the compensation circuit includes a storage circuit for storing the output signal of the second pixel and a differential amplifier circuit for outputting a difference between the output signal of the first pixel and the output signal of the second pixel stored in the storage circuit.

15. (Original) A solid-state image-sensing device comprising:

a first pixel including a photoelectric conversion element and capable of generating selectively either an output signal that is logarithmically proportional to an amount of light incident on the photoelectric conversion element or an output signal that is linearly proportional to the amount of light incident on the photoelectric conversion element;

a second pixel for generating as an output signal a compensation signal with which to compensate the output signal of the first pixel; and

a reading circuit for reading out the output signals of the first and second pixels.

16. (Previously Presented) A solid-state image-sensing device comprising:

a first pixel, which includes a photoelectric conversion element, for generating a first pixel output signal that is logarithmically proportional to an amount of light incident on the photoelectric conversion element;

a second pixel for generating a second pixel output signal,

wherein the second pixel output signal is used for reducing signal noise that is caused by the first pixel; and

a reading circuit for reading out the output signals of the first and second pixels.

17. (Previously Presented) A solid-state image-sensing device as claimed in claim 16, further comprising a memory for storing the second pixel output signal.

18. (Previously Presented) A solid-state image-sensing device as claimed in claim 16, wherein the signal noise caused by the first pixel is a result of a switching action of at least one semiconductor device included therein.

19. (Previously Presented) A solid-state image-sensing device as claimed in claim 18, wherein the signal noise caused by the first pixel is a result of a transistor being turned off.

20. (Previously Presented) A solid-state image-sensing device as claimed in claim 16, wherein the signal noise caused by the first pixel is a result of the first pixel being reset.

21. (Previously Presented) A solid-state image sensing device comprising:

a first pixel including a photoelectric conversion element and capable of generating an output signal that is logarithmically proportional to an amount of light incident on the photoelectric conversion element;

a reading circuit for reading out the output signal of the first pixel; and

a second pixel for generating a compensation signal with which to compensate for a variation ascribable to a characteristic of the reading circuit.

22. (Previously Presented) A solid-state image-sensing device as claimed in claim 21, wherein the characteristic of the reading circuit is an amplification factor thereof.

23. (Previously Presented) A solid-state image-sensing device as claimed in claim 21, wherein the reading circuit is a transistor.

RESPONSE TRANSMITTAL AND FEE AUTHORIZATION

ATTORNEY DOCKET NO.: 15162/03810			APPLICATION NO.: 09/896,573	
FILING DATE: June 29, 2001	CONFIRMATION NO: 7850	CUSTOMER NO. 24367	EXAMINER: Stephone B. Allen	GROUP ART UNIT 2878
INVENTOR(S): Yoshio HAGIHARA				
TITLE OF INVENTION: SOLID-STATE IMAGE-SENSING DEVICE				

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April 22, 2004
Date of Deposit

Brian E. Harris
Name of Applicant, Assignee, or Registered Representative

Signature

April 22, 2004
Date of Signature

TRANSMITTED HEREWITH FOR THE ABOVE IDENTIFIED PATENT APPLICATION IS:

- ☐ (A) A response to the Office Action dated:
- ☐ (B) A Petition for Extension of Time
  - ☐ for 1 month ☐ for 2 months ☐ for 3 months;
  - A Petition for Extension of Time, having been previously filed,
  - ☐ for 1 month ☐ for 2 months ☐ for 3 months
- ☐ (C) A Notice of Appeal. $
- ☒ (D) An Appellant's Brief on Appeal. $330.00
- ☐ (E) Other: . $
- ☐ (F) A verified statement to establish small entity status under 37 CFR §§ 1.9 and 1.27
- ☐ Small entity status under 37 CFR § 1.27 has been previously established
- ☐ The claims fee, if any, has been calculated as shown below

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA
TOTAL		MINUS		
INDEP.		MINUS		
FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

SMALL ENTITY			LARGE ENTITY	
RATE	ADD'L FEE	OR	RATE	ADD'L FEE
x $9	$		x $18	$
x $43			x $86	
+ $145			+ $290	
TOTAL ADD'L FEE	$ 0.00		TOTAL ADD'L FEE	$ 0.00

- ☒ Please charge $330.00 to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260, which includes
  - ☐ the amount of $ for the claims fee calculated above AND/OR
  - ☒ the amount of $330.00 for the fee for item(s) ☐ (B) ☐ (C) ☒ (D) ☐ (E) ☐ (F)
- ☒ Please charge any additional fees (other than issue fee) required during the pendency of this application to Deposit Account No. 18-1260. Please credit any overpayment to Deposit Account No. 18-1260.
- ☒ A duplicate copy of this Response Transmittal and Fee Authorization is enclosed.

April 22, 2004
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